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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	3442US (96-428)
First Inventor or Application Identifier	Salman Akram
Title	METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME
Express Mail Label No.	EL312579894US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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2. [X] Specification [*Total Pages* 29] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 14]
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   - b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
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8. [X] Assignment Papers (cover sheet & document(s))
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[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* [X] *Correspondence address below*

Name	Joseph A. Walkowski Trask, Britt & Rossa				
Address	P.O. Box 2550				
City	Salt Lake City	*State*	Utah	*Zip Code*	84110
Country	USA	*Telephone*	(801) 532-1922	*Fax*	(801) 531-9168

Name (Prnt/Type)	Joseph A. Walkowski	*Registration No. (Attorney/Agent)*	28,765
Signature		*Date*	09/01/99

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APPLICATION FOR LETTERS PATENT

for

METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

Inventor:
Salman Akram

Attorney:
Joseph A. Walkowski
Registration No. 28,765
Trask, Britt, & Rossa
P.O. Box 2550
Salt Lake City, Utah 84110

METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

BACKGROUND OF THE INVENTION

Field of the Invention: This invention relates generally to the field of semiconductor device design and fabrication. Specifically, the invention relates to methods for manufacturing metallization structures in integrated circuit devices and the resulting structures.

State of the Art: Integrated circuits (ICs) contain numerous individual devices, such as transistors and capacitors, that are interconnected by an intricate network of horizontal and vertical conductive lines commonly termed interconnects. Exemplary interconnect structures are disclosed in U.S. Patent Nos. 5,545,590, 5,529,954, 5,300,813, 4,988,423, and 5,356,659, each of which patents is hereby incorporated herein by reference.

Aluminum interconnect structures are decreasing in size and pitch (spacing), as the industry trend continues to, and including, submicron features pitches. The resultant reduction in structure sizes leads to numerous reliability concerns, including electromigration and stress voiding of the interconnect structures.

Stress notches (also known as stress voids) on the surface of conductive interconnect structures are of concern because the voids or notches degrade reliability and device performance. Stress notches, when formed in a conductive line, may render the line substantially discontinuous and unable to effectively transmit a signal. Stress notches at a grain boundary are extremely detrimental, as they may propagate along the boundary and sever the conductive line completely.

Stress notches are also undesirable because they can alter the resistivity of a conductive line and change the speed at which signals are transmitted. Resistivity changes from stress notching are especially important as line dimensions shrink, because notching in a submicron conductive line alters resistivity more than notching in a larger line with its consequently greater cross-sectional area. Thus, the ever more stringent

pitch sizing and higher aspect ratios (height to width of the structure or feature) sought by practitioners in the art have imitated considerable stress voiding concerns.

It is believed that stress notching results from both structural and thermal stresses between conductive lines and adjacent insulating and passivation layers. Kordic et al., *Size and Volume Distributions of Thermally Induced Stress Voids in AlCu Metallization*, Appl. Phys. Lett., Vol. 68, No. 8, 19 February 1996, pp. 1060-1062, incorporated herein by reference, describes how stress voids begin at the edge of a conductive line where the density of the grain boundaries is largest. As illustrated in Figure 12 herein, stress notches form at the exterior surfaces and surface intersections of the conductive lines in order to relieve areas of high stress concentration. The notches may then propagate into, and across, the interior of the conductive line until the line becomes disrupted, cracked, and/or discontinuous.

Aluminum (Al) and Al alloy (such as Al/Cu) lines are especially susceptible to stress notching because of both the thermal expansion mismatch between Al and adjacent layers and the relatively low melting point of Al. As the temperature changes, stresses are induced in Al or Al alloy lines because aluminum's coefficient of thermal expansion (CTE) differs from the CTE of the materials comprising the adjacent layers. To relieve these stresses, Al atoms migrate and form stress notches. Further, because Al has a low melting point, Al atoms migrate easily at low temperatures and aggravate a tendency toward stress notch formation.

Several methods have been proposed to reduce stress notching. One proposed method uses a material less susceptible to stress notching, such as copper (Cu) or tungsten (W), in the conductive line. Using Cu in conductive lines, however, has in the past resulted in several problems. First, copper is difficult to etch. Second, adhesion between copper and adjacent insulating layers is poor and thus poses reliability concerns. Third, adding Cu to Al lines may reduce stress notching, but beyond a certain Cu concentration, device performance may begin to degrade. Fourth, as conductive line geometries shrink, adding Cu to Al lines seems less effective in reducing stress notching. Finally, even using Cu interconnects in the manner employed in the prior art can still lead

to notching effects, especially at 0.1 μm geometries and below since, at such dimensions, line widths have become so small that any imperfection can cause opens. Using W in Al conducting lines is also undesirable – W has a high resistivity, and therefore reduces signal speed.

Another proposed method to reduce stress notching modifies how the layers adjacent conductive lines (e.g., insulating and passivation layers) are formed. This method has focused, without notable success, on the rate, temperature, and/or pressure at which the adjacent layers are deposited, as well as the chemical composition of such layers.

Yet another proposed method to reduce stress notching comprises forming a cap on the conductive lines. Such caps can be formed from TiN, W, or Ti-W compounds. These materials have higher melting points than Al and, therefore, have a higher resistance to stress notching. A disadvantage in using such caps, however, is that additional process steps, such as masking steps, are required.

U.S. Patent No. 5,317,185, incorporated herein by reference, describes still another proposed method for reducing stress notching. This patent discloses a IC device having a plurality of conductive lines, where the outermost conductive line is a stress–reducing line. This stress–reducing line is a non-active structure which reduces stress concentrations in the inner conductive lines.

SUMMARY OF THE INVENTION

The present invention relates to a metallization structure for semiconductor device interconnects comprising a substrate having a substantially planar upper surface, a metal layer disposed on a portion of the substrate upper surface, a conducting layer overlying the metal layer, and metal spacers flanking the sidewalls of the conducting layer and the underlying metal layer. The metal layer and metal spacers do not encapsulate the conducting layer. The substrate upper surface is preferably a dielectric layer. The conducting layer preferably comprises aluminum or an aluminum-copper alloy, but may also comprise copper. When the conducting layer comprises Al, the metal layer and

metal spacer preferably comprise titanium, such as Ti or TiN. An optional dielectric layer, preferably silicon oxide, may be disposed on the conducting layer. When the optional dielectric layer is present, the metal spacer extends along the sidewall of the dielectric layer.

The present invention also relates to a metallization structure comprising a substrate having a metal layer disposed thereon, a dielectric layer having an aperture therethrough disposed on the substrate so the bottom of the aperture exposes the upper surface of the metal layer, at least one metal spacer on the sidewall of the aperture, and a conducting layer filling the remaining portion of the via. The metal layer and metal spacer preferably comprises titanium, such as Ti or TiN. At least one upper metal layer may be disposed on the conducting layer.

The present invention further relates to a method for making a metallization structure by forming a substantially planar first dielectric layer on a substrate, forming a metal layer over the first dielectric layer, forming a conducting layer over the metal layer, forming a second dielectric layer over the conducting layer, removing a portion of the second dielectric layer, conducting layer, and metal layer to form a multi-layer structure, and forming metal spacers on the sidewalls of the multi-layer structure. The process optionally removes both the second dielectric layer portion of the multi-layer structure and the laterally adjacent portions of the metal spacers.

The present invention additionally relates to a method for making a metallization structure by forming a substrate comprising a metal layer disposed thereon, forming a dielectric layer comprising an aperture on the substrate so the bottom of the aperture exposes the upper surface of the metal layer, forming a metal spacer on the sidewall (in the case of a via) or sidewalls (in the case of a trench) of the aperture, and forming a conducting layer in the remaining portion of the via. At least one upper metal layer may optionally be formed on the conducting layer.

The present invention also relates to a method for making a metallization structure by forming a substrate comprising a metal layer on the surface thereof,

forming on the substrate a dielectric layer comprising an aperture so the bottom of the aperture exposes the surface of the metal layer, forming a conducting layer in the aperture, forming an upper metal layer overlying the dielectric layer and the aperture, removing the portions of the upper metal layer overlying the dielectric layer, removing the dielectric layer, removing the portions of the metal layer not underlying the aperture to form a multi-layer metal structure, and forming a metal spacer on the sidewall or sidewalls of the multi-layer metal structure.

The present invention provides several advantages when compared to the prior art. One advantage is that thermally-induced stress voids are reduced because the metal layer and metal spacer comprise materials exhibiting good thermal-voiding avoidance characteristics. Another advantage is that the size of conductive lines can be shrunk further in comparison to dimensions achievable by conventional processes, since only one additional deposition and etch step, without an additional masking step, is needed to form the metallization structure. Shrinking of conductive lines is necessary as device geometries decrease to less than 0.1 μm, At these small geometries, even small notches can significantly decrease conductivity.

The invention also specifically includes semiconductor devices including the inventive metallization structures.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention, in part, is illustrated by the accompanying drawings in which:

Figures 1, 2, 3a, and 3b illustrate cross-sectional views of one process of forming a metallization structure, and the structure formed thereby, according to the invention;

Figures 4, 5, 6, 7a, and 7b illustrate cross-sectional views of another process of forming a metallization structure, and the structure formed thereby, according to the invention;

Figures 8 and 9 illustrate cross-sectional views of yet another process of forming a metallization structure, and the structure formed thereby, according to the invention;

Figures 10 and 11 illustrate cross-sectional views of still another process of forming a metallization structure, and the structure formed thereby, according to the invention; and

Figure 12 illustrates a partial cross-sectional, perspective view of a conventional, prior art metallization structure exhibiting stress voids or notches.

DETAILED DESCRIPTION OF THE INVENTION

Generally, the present invention relates to a metallization structure for interconnects and semiconductor devices including same. Specifically, the present invention reduces stress voiding, especially thermally-induced stress voiding, in conducting lines. The metallization structures described below exemplify the present invention without reference to a specific device because the inventive process and structure can be modified by one of ordinary skill in the art for any desired device.

The following description provides specific details, such as material thicknesses and types, in order to provide a thorough description of the present invention. The skilled artisan, however, would understand that the present invention may be practiced without employing these specific details. Indeed, the present invention can be practiced in conjunction with conventional fabrication techniques employed in the industry.

The process steps described below do not form a complete process flow for manufacturing IC devices. Further, the metallization structures described below do not form a complete IC device. Only the process steps and structures necessary to understand the present invention are described below.

One embodiment of a process and resulting metallization structure of the present invention is illustrated in Figures 1, 2, 3a, and 3b. This embodiment may be characterized as a predominantly "subtractive" process, in comparison to the second embodiment discussed hereinafter, in that portions of superimposed material layers are removed to define the interconnect structure features, such as lines. As shown in Figure 1, a portion of semiconductor device 2 includes substrate 4 with overlying first dielectric layer 6. Substrate 4 may be any surface suitable for integrated circuit device formation,

such as a silicon or other semiconductor wafer or other substrate, and may be doped and/or include an epitaxial layer. Substrate 4 may also be an intermediate layer in a semiconductor device, such as a metal contact layer or an interlevel dielectric layer. Preferably, substrate 4 is a silicon wafer or bulk silicon region, such as a silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) structure.

First dielectric layer 6 may comprise any dielectric material used in IC device fabrication. Examples of such dielectric materials include silicon oxide, silicon nitride, silicon oxynitride, silicon oxide containing dopants such as boron (B) or phosphorus (P), organic dielectrics, or a layered dielectric film of these materials. Preferably, first dielectric layer 6 is silicon oxide or borophosphosilicate glass (BPSG). First dielectric layer 6 may be formed by any process yielding the desired physical and chemical characteristics, such as thermal oxidation, thermal nitridation, or vapor deposition.

Overlying first dielectric layer 6 is metal layer 8. One or more individual metal layers may be used as metal layer 8. For example, if two superimposed metal layers are employed (represented by the dashed line in metal layer 8), an adhesion-promoting metal layer can be a first, lower portion of metal layer 8 on dielectric layer 6 and a stress reducing layer can be a second, upper portion of metal layer 8. Other metal layers might be included for other functions, such as a layer for reducing electromigration. Preferably, a single metal layer is used as metal layer 8, especially when the single layer can reduce electromigration, function as an adhesion promoting layer, and function as a stress reducing layer. If two metal layers are employed, the first, upper metal layer may, for example, comprise tantalum, titanium, tungsten, TaN, or TiN and the second, lower metal layer overlying dielectric layer 6 may, for example, comprise TiN, TiW, WN, or TaN.

Metal layer 8 includes not only metals, but their alloys and compounds (e.g., nitrides and silicides). For example, a metal layer containing titanium might also contain nitrogen or silicon, such as titanium nitride or titanium silicide. Any metal, metal alloy, or metal compound can be employed in metal layer 8, provided it exhibits the characteristics described above, either alone or when combined with other metal layers. Examples of metals that can be employed in metal layer 8 include cobalt (Co), Ti, W, Ta,

molybdenum (Mo), and alloys and compounds thereof, such as TiW or TiN. Preferably, metal layer 8 comprises titanium. Titanium is a good adhesion layer and serves as a stress reducing layer since Ti exhibits good thermal voiding resistance characteristics.

Metal layer 8 is deposited or otherwise formed by any process used in IC device fabrication. For example, metal layer 8 may be deposited by chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques, depending on the characteristics required of the layer. As used herein, the term "CVD techniques" encompasses, without limitation, plasma-enhanced CVD, or PECVD. Preferably, when metal layer 8 is Ti, this layer is formed by sputtering (a form of PVD) a film of Ti. If metal layer 8 is a metal nitride, it may be formed, for example, by depositing the metal in a nitrogen-containing atmosphere or by depositing the metal and annealing in a nitrogen-containing atmosphere. If metal layer 8 is a metal silicide, it may be formed, for example, by first depositing either the metal layer or a silicon layer, then depositing the other, and heating to react the two layers and form the silicide. If metal layer 8 is a metal alloy, it may be formed by any process suitable for depositing the metal alloy. For example, either sputtering or CVD techniques can be employed.

Conducting layer 10 is then formed over metal layer 8. Conducting layer 10 may comprise any conducting material used in IC device fabrication. Preferably, conducting layer 10 comprises a conducting metal, such as Al, optionally containing other elements such as Si, W, Ti, and/or Cu. More preferably, conducting layer 10 is an aluminum-copper alloy. Conducting layer 10 may also be formed of Cu. Conducting layer 10 may be formed by any method used in IC device fabrication such as CVD or PVD techniques. Preferably, conducting layer 10 is deposited by a PVD method such as sputtering, as known in the art. Second dielectric layer 12 is next deposited or otherwise formed on top of conducting layer 10. Second dielectric layer 12 comprises any dielectric material used in IC device fabrication, including those listed above. Preferably, second dielectric layer 12 comprises a material that serves as an etch stop, as explained below. More preferably, dielectric layer 12 comprises fluorine-doped silicon oxide or other low dielectric constant material. Second dielectric layer 12 may be formed by any suitable process giving the

desired physical and chemical characteristics, such as CVD, PECVD (plasma enhanced chemical vapor deposition, spin-on methods, or otherwise, depending upon the dielectric material selected. For use of the preferred fluorine-doped silicon oxide, the preferred deposition method is PECVD.

As shown in Figure 2, a portion of second dielectric layer 12, conducting layer 10, and metal layer 8 have been removed, forming multi-layer structure 13. The portions of layers 8, 10 and 12 are removed by any IC device fabrication process, such as a photolithographic patterning and dry etching process. The resulting multi-layer structure forms the basis for an interconnect structure according to the present invention. Of course, the patterning and etch process would normally be performed to define a large number of interconnect structures, such as conductive lines 100 (see Figures 3a and 3b) extending across substrate 4.

As also shown in Figure 2, second metal layer 14 (also termed a metal spacer layer) is then deposited on first dielectric layer 6 and over multi-layer structure 13. In similar fashion to the structure of metal layer 8, one or more individual metal layers, illustrated by the dashed line within metal layer 14, may be used as metal layer 14. Preferably, a single metal layer is used as metal layer 14 for the same reasons as those set forth for metal layer 8.

Like metal layer 8, metal layer 14 includes not only metals, but their alloys and compounds (e.g., nitrides and silicides). Preferably, when conducting layer 12 comprises aluminum , metal layer 14 comprises Ti. If conducting layer 10 comprises Cu, metal layer 14 preferably comprises TiW. More preferably, metal layer 14 comprises the same metal as first metal layer 8. Metal layer 14 may be deposited or otherwise formed by a process similar to the process used to form metal layer 8. Preferably, metal layer 14 is formed by a conformal deposition process, such as CVD.

Next, as illustrated in Figure 3a, metal layer 14 is spacer etched to remove portions of the metal layer 14 on first dielectric layer 6 and the second dielectric layer 12, thereby leaving spacers 16 on the multi-layer structure 13. A spacer etch is a directional sputtering etch which removes metal layer 14 so that spacers 16 remain on the sidewalls

of multi-layer structure 13. The spacer etch uses the first and second dielectric layers as an etch stop.

If desired, second dielectric layer 12 can then be removed. Second dielectric layer 12 can be removed by any process which removes the second dielectric layer without removing first dielectric layer 6. If the first and second dielectric layers comprise different materials (e.g., when second dielectric layer 12 is silicon oxide and the first dielectric layer 6 is BPSG), any process which selectively etches the second dielectric layer 12 can be employed. The etch process would also remove the portions of sidewalls 16 laterally adjacent dielectric layer 12, thus resulting in the metallization structure illustrated in Figure 3b. When the first and second dielectric layers are similar or have similar etch rates, (e.g., when both are silicon oxide or fluorine-doped), a facet etch process can be used. As shown in broken lines in Figure 3b, when the first and second dielectric layers 6 and 12 exhibit similar etch rates, the thickness of layer 6 will be reduced by substantially the thickness of removed layer 12.

The metallization structures illustrated in Figures 3a and 3b reduce thermally-induced stress voids in conductive lines 100. Metal layer 8 and metal spacers 16 serve as a protective coating at the respective lower and lateral surfaces of conductive lines 100 and at intersections thereof, thereby reducing the incidence of stress voids by preventing them from starting at these surfaces and intersections thereof on conductive line 100. Metal layer 8 and metal spacers 16 also increase reliability of conductive line 10 without reducing its resistance.

The metallization structures of Figures 3a and 3b can then be processed as desired to complete the IC device. For example, an interlevel dielectric layer could be deposited thereover, contact or via holes could be cut in the interlevel dielectric, a patterned metal layer could be formed to achieve a desired electrical interconnection pattern, and a protective dielectric overcoat deposited and patterned to expose desired bond pads.

Another embodiment of a process and resulting metallization structures of the present invention is represented in Figures 4 through 11. This embodiment may be characterized as more of an "additive" method or process than that described with respect

to Figures 1 through 3, in that metallization structures for interconnects are formed by deposition in apertures, such as vias or trenches. As such, it should be noted that cusping of material deposited to line the sidewall or sidewalls of an aperture may be of concern if the method of deposition is not sufficiently anisotropic or, in some instances, the aperture exhibits a very high aspect ratio. In Figure 4, metal layer 52 has been deposited or otherwise formed over substrate 50. Any of the substrates employable as substrate 4 above can be used as substrate 50. Preferably, substrate 50 is a silicon wafer or bulk silicon region, such as an SOI or SOS structure. Such substrate 50 can have active and passive devices and other electrical circuitry fabricated on it, these circuit structures being interconnected by the metallization structures of the present invention. Therefore, a direct electrical path may exist between the devices and circuitry of the substrate 50 (or 4), the devices and circuitry being omitted herein for simplicity.

Metal layer 52 may comprise a discrete conductive member, such as a wire, a stud, or a contact. Preferably, metal layer 52 is substantially similar to metal layer 8 described above and may be of any of the same metals, alloys or compounds. If desired, a dielectric layer 51 can be formed on substrate 50 and beneath metal layer 52. Dielectric layer 51 is substantially similar to dielectric layer 6 described above.

As illustrated in Figure 4, dielectric layer 54 is then deposited or otherwise formed on metal layer 52. Dielectric layer 54 may be any dielectric or insulating material used in IC device fabrication, such as such as those listed above for dielectric layer 12. Preferably, dielectric layer 54 is silicon oxide or spin on glass (SOG). Dielectric layer 54 may be formed by any IC device fabrication process giving the desired physical and chemical characteristics.

An aperture such as a via or trench 56 is then formed in dielectric layer 54 by removing a portion of dielectric layer 54 to expose underlying metal layer 52. Aperture 56 may be formed by any IC device manufacturing method, such as a photolithographic patterning and etching process.

As shown in Figure 5, metal collar 60 is formed on the sidewalls of aperture 56, using a spacer etch as known in the art. It will be understood that the term "collar"

encompasses a co-parallel spacer structure 60 if aperture 56 is a trench extending over substrate 50. Similar to metal layer 14, collar 60 may contain one or more metal layers with a single metal layer preferably used. Also in similar fashion to metal layer 14, collar 60 may include not only metals, but their alloys and compounds. Like metal layer 14, any metal can be employed in collar 60, provided it exhibits the desired characteristics, either alone or when combined with other metal layers, and the metals applicable to metal layer 14 are equally applicable to collar 60. Preferably, collar 60 comprises the same metal as conducting layer 52. More preferably, when conductive layer 52 comprises Al, collar 60 comprises Ti.

Collar 60 is formed by an IC device fabrication process which does not degrade metal layer 52, yet forms a collar or spacer-like structures 60 on the sidewall or sidewalls of aperture 56. For example, layer 61 (shown in Figure 4) of a material from which collar 60 is formed can be conformally deposited on dielectric layer 54 and the walls of via 56. Conformal coverage yields a substantially vertical sidewall in the dielectric aperture. While not preferred, a partially conformal layer of the material can be deposited instead. A highly conformal process is preferably employed to form layer 61. Portions of layer 61 on the bottom of via 56 and top of dielectric layer 54 are then removed, preferably by using an appropriate directional etch, such as reactive ion etching (RIE).

Conducting layer 62 is next deposited or otherwise formed to fill aperture 56 and extend over dielectric layer 54, as shown in broken lines in Figure 5. Conducting layer 62 may be deposited by any IC device fabrication method yielding the desired characteristics. For example, conducting layer 62 may be deposited by a conformal or non-conformal deposition process. An abrasive planarization process, such as chemical-mechanical planarization (CMP), is then used to remove portions above the horizontal plane of the upper surface of dielectric layer 54 and leave conductive plug (in a via 56) or line (in a trench 56) 64 as illustrated in Figure 6.

Similar to conducting layer 10, conducting layer 62 comprises any conducting material used in IC devices. Preferably, conducting layer 62 comprises aluminum, optionally containing other metals such as Si, W, Ti, and/or Cu. More preferably,

conducting layer 62 is an aluminum-copper alloy. Conducting layer 62 may also comprise copper metal.

Dielectric layer 54 can then be optionally removed, thus forming the interconnect structure represented in Figure 7a. Dielectric layer 54 can be removed by any process which does not degrade any of metal layer 52, conductive layer 62, or collar 60. For example, when dielectric layer 54 is silicon oxide, it may be removed by an HF wet etch solution or an oxide dry etch process. If desired, portions of metal layer 52 can then be removed, preferably by a directional etching process, to obtain the interconnect structure shown in Figure 7b.

In an alternative method, upper metal layer 66 can be formed over conductive plug or line 64 as depicted in Figure 8. Like metal layer 52, upper metal layer 66 may contain one or more individual metal layers. Preferably, a single metal layer is used as upper metal layer 66. Similar to metal layer 52, upper metal layer 66 may contain not only metals, but their alloys and compounds. Preferably, metal layer 66 comprises the same material as collar 60. More preferably, when conductive plug 64 comprises Al, metal layer 66 comprises Ti.

Upper metal layer 66 can be formed over conductive plug 64 in the following manner. Conductive layer 62 is deposited in aperture 56 and over dielectric layer 54 as described above with respect to Figure 5. Prior to completely filling aperture 56, however, the deposition of conductive layer 62 is halted as shown at 62a in Figure 5, leaving an upper portion of aperture 56 empty (i.e, a recess is left at the top of aperture 56). Upper metal layer 66 is then deposited over conductive layer 62, including the still-empty upper portion of aperture 56. Portions of conductive layer 62 and upper metal layer 66 above the horizontal plane of dielectric layer 54 are then removed by a planarization process, such as CMP, to form a completely enveloped, or clad, interconnect structure. If desired, portions of dielectric layer 54 and metal layer 52 flanking the interconnect structure can be removed as described above to form the structure of Figure 9.

In another process, variant after forming metal layer 52 on substrate 50 and forming dielectric layer 54 with aperture 56 therethrough, but prior to forming collar 60, conductive plug or line 64 could be formed in aperture 56 as described above. Upper metal layer 66 could then be deposited, as described above, over conductive plug or line 64 and dielectric layer 54 to obtain the structure illustrated in Figure 10. Portions of upper metal layer 66 not overlying conductive plug or line 64 could then be removed by a photolithographic pattern and etch process, followed by removing dielectric layer 54 by the method described above, to obtain the structure illustrated in Figure 11. As explained above, the structure of Figure 11 could then have a conformed metal layer deposited and etched (similar to the deposition and etch of metal layer 14 above) to form a structure similar to that depicted in Figure 3a.

While the preferred embodiments of the present invention have been described above, the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A metallization structure for a semiconductor device, comprising:

a substrate comprising a substantially planar upper surface;

a metal layer defining a pattern on a portion of the substrate upper surface;

a conducting layer overlying and substantially coextensive with the metal layer, said metal layer and said conducting layer having substantially aligned sidewalls; and

metal spacers flanking the sidewalls of the conducting layer and metal layer.

2. The metallization structure of claim 1, further comprising a dielectric layer on the substrate upper surface and underlying the metal layer.

3. The metallization structure of claim 2, wherein the dielectric layer is silicon oxide or BPSG.

4. The metallization structure of claim 1, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

5. The metallization structure of claim 4, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

6. The metallization structure of claim 5, wherein the first metal layer comprises titanium or titanium nitride.

7. The metallization structure of claim 1, wherein the metal layer is titanium or titanium nitride.

8. The metallization structure of claim 1, wherein the conducting layer is selected from the group comprising aluminum and copper.

9. The metallization structure of claim 8, wherein the conducting layer is an aluminum-copper alloy.

10. The metallization structure of claim 1, wherein the metal spacers comprise at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

11. The metallization structure of claim 11, wherein the metals spacers are titanium or titanium nitride.

12. The metallization structure of claim 1, further comprising a dielectric layer on the conducting layer and having sidewalls aligned therewith, the metal spacers extending along the sidewalls of the dielectric layer.

13. The metallization structure of claim 12, wherein the dielectric layer comprises a low dielectric constant material.

14. The metallization structure of claim 13, wherein the dielectric layer is fluorine-doped silicon oxide.

15. The metallization structure of claim 1, wherein the metal layer and the metal spacers comprise the same metal.

16. A metallization structure for a semiconductor device, comprising:
a substrate having a metal layer disposed thereon;

a dielectric layer having an aperture therethrough defined by at least one sidewall and exposing the metal layer;

a metal spacer on the at least one sidewall of the aperture; and

a conductive layer substantially filling a remaining portion of the aperture.

17. The metallization structure of claim 16, wherein the metal layer comprises tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN.

18. The metallization structure of claim 17, wherein the metal layer is titanium or titanium nitride.

19. The metallization structure of claim 16, wherein the at least one metal spacer includes at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN.

20. The metallization structure of claim 19, wherein the at least one metal spacer is titanium or titanium nitride.

21. The metallization structure of claim 16, wherein the substrate comprises a dielectric layer underlying the metal layer.

22. The metallization structure of claim 21, wherein the dielectric underlying the metal layer is silicon oxide or BPSG.

23. The metallization structure of claim 16, wherein the metal layer and the at least one metal spacer comprise the same metal.

24. The metallization structure of claim 16, wherein the metal layer is a first metal layer comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

25. The metallization structure of claim 24, further including a second metal layer disposed between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

26. The metallization structure of claim 16, further comprising at least one upper metal layer on the conductive layer and comprising Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

27. The metallization structure of claim 26, wherein the at least one upper metal layer comprises a plurality of upper metal layers.

28. The metallization structure of claim 16, wherein the at least one upper metal layer comprises titanium or titanium nitride.

29. A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal layer over the first dielectric layer;

forming a conducting layer over the metal layer;

forming a second dielectric layer over the conducting layer;

removing aligned portions of the second dielectric layer, conducting layer, and metal layer to form a multi-layer structure; and

forming metal spacers on sidewalls of the multi-layer structure.

30. The method of claim 29, wherein forming the first dielectric layer comprises forming a silicon oxide or BPSG layer.

31. The method of claim 29, further including forming the at least one metal layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

32. The method of claim 31 further including forming a second metal layer between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

33. The method of claim 29, further including forming the at least one metal layer of titanium or titanium nitride.

34. The method of claim 29, wherein the at least one metal layer is a single metal layer and further comprising forming the single metal layer of titanium or titanium nitride.

35. The method of claim 29, further comprising forming the conducting layer from the group comprising aluminum and copper.

36. The method of claim 35, further including forming the conducting layer of an aluminum-copper alloy.

37. The method of claim 29, further including forming the metal spacers of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

38. The method of claim 37, further including forming the metal spacers of titanium or titanium nitride.

39. The method of claim 29, further comprising forming a dielectric layer on the conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal spacers to extend along the sidewalls of the dielectric layer.

40. The method of claim 39, further comprising forming the dielectric layer of a low dielectric constant material.

41. The method of claim 40, further comprising forming the dielectric layer of a fluorine-doped silicon oxide.

42. The method of claim 29, further comprising forming the at least one metal layer and the metal spacers of the same metal.

43. The method of claim 29, further comprising forming the at least one metal layer by vapor deposition.

44. The method of claim 42, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

45. The method of claim 29, further comprising forming the conducting layer by vapor deposition.

46. The method of claim 45, further comprising forming the conducting layer by CVD, PVD or PECVD.

47. The method of claim 29, further comprising forming the metal spacers by vapor deposition and directional etching.

48. The method of claim 47, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

49. The method of claim 29, wherein removing aligned portions of the second dielectric layer, conducting layer, and metal layer to form a multi-layer structure is effected by patterning and etching the second dielectric layer, the conducting layer, and the metal layer.

50. The method of claim 29, further comprising forming the metal spacers by forming a metal spacer layer over the multi-layer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

51. The method of claim 50, further comprising forming the metal spacer layer over the multi-layer structure and first dielectric layer by a conformal deposition process.

52. The method of claim 51, wherein the portions of the metal layer over the multi-layer structure and first dielectric layer are removed by etching.

53. The method of claim 29, further comprising:
removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto.

54. The method of claim 53, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal spaces by etching.

55. A method for making a metallization structure comprising:
forming a substrate comprising at least one metal layer on the surface thereof;
forming a dielectric layer over at least one the metal layer;

forming an aperture having at least one sidewall through the dielectric layer to expose a surface of the at least one metal layer;

forming a metal spacer on the at least one sidewall of the aperture; and

forming a conductive layer in a remaining portion of the aperture.

56. The method of claim 55, further comprising forming the dielectric layer of silicon oxide.

57. The method of claim 55, further including forming the at least one metal layer of Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

58. The method of claim 57, wherein the at least one metal layer comprises a first metal layer, and further including forming a second metal layer between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

59. The method of claim 55, further including forming the at least one metal layer of titanium or titanium nitride.

60. The method of claim 55, further comprising forming the at least one metal layer by vapor deposition.

61. The method of claim 60, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

62. The method of claim 55, further comprising forming the conducting layer by vapor deposition.

63. The method of claim 62, further comprising forming the conducting layer by CVD, PVD or PECVD.

64. The method of claim 55, further comprising forming the at least one metal layer and the metal spacer of the same metal.

65. The method of claim 55, further comprising forming the metal spacer by vapor deposition and directional etching.

66. The method of claim 55, further including forming the metal spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys or compounds thereof, including TaN or TiN.

67. The method of claim 66, further including forming the metal spacer of titanium or titanium nitride.

68. The method of claim 55, further comprising forming at least one upper metal layer on the conductive layer.

69. The method of claim 68, further comprising forming the at least one upper metal layer on the conductive layer from Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

70. The method of claim 68, further comprising forming the at least one upper metal layer as a plurality of upper metal layers.

71. The method of claim 68, further comprising forming the at least one upper metal layer of titanium or titanium nitride.

72. The method of claim 68, further comprising forming the at least one upper metal layer by vapor deposition.

73. The method of claim 72, wherein the vapor deposition is effected by CVD, PVD or PECVD.

74. The method of claim 55, further comprising removing the dielectric layer and portions of the at least one metal layer not underlying the aperture.

75. The method of claim 74, further comprising removing the dielectric layer by using a hydrofluoric acid wet etch solution or an oxide dry etch process.

76. The method of claim 74, further comprising removing the portions of the at least one metal layer by directional etching.

77. A method for making a metallization structure comprising:

forming a substrate comprising at least one metal layer on the surface thereof;

forming a dielectric layer over the at least one metal layer;

forming an aperture through the dielectric layer to expose a surface of the at least one metal layer;

forming a conducting layer in the aperture;

forming at least one upper metal layer overlying the dielectric layer and the conducting layer in the aperture;

removing portions of the at least one upper metal layer overlying the dielectric layer, removing the dielectric layer, and removing portions of the at least one metal layer surrounding the conducting layer to form a multi-layer metal structure having at least one sidewall; and

forming a metal spacer on the at least one sidewall of the multi-layer metal structure.

78. The method of claim 77, further comprising forming the dielectric layer of silicon oxide.

79. The method of claim 77, further including forming the at least one metal layer of Ti, Ta, W, Co or Mo or alloys or compounds thereof, including TaN or TiN.

80. The method of claim 79, wherein the at least one metal layer comprises a first metal layer, and further including forming a second metal layer between the first metal layer and the substrate and comprising TiN, TiW, WN, or TaN.

81. The method of claim 77, further including forming the at least one metal layer of titanium or titanium nitride.

82. The method of claim 77, further comprising forming the at least one metal layer by vapor deposition.

83. The method of claim 82, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

84. The method of claim 77, further comprising forming the conducting layer by vapor deposition.

85. The method of claim 84, further comprising forming the conducting layer by CVD, PVD or PECVD.

86. The method of claim 77, further comprising forming the at least one metal layer and the metal spacer of the same metal.

87. The method of claim 77, further comprising forming the metal spacer by vapor deposition of a metal layer over the multi-layer metal structure and directional etching of the vapor-deposited metal layer.

88. The method of claim 77, further including forming the metal spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN or TiN.

89. The method of claim 88, further including forming the metal spacer of titanium or titanium nitride.

90. The method of claim 77, further comprising forming the at least one upper metal layer on the conducting layer from Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

91. The method of claim 90, further comprising forming the at least one upper metal layer as a plurality of upper metal layers.

92. The method of claim 77, further comprising forming the at least one upper metal layer of titanium or titanium nitride.

93. The method of claim 77, further comprising forming the at least one upper metal layer by vapor deposition.

94. The method of claim 93, wherein the vapor deposition is effected by CVD, PVD or PECVD.

95. The method of claim 77, further comprising removing the dielectric layer by using a hydrofluoric acid wet etch solution or an oxide dry etch process.

96. The method of claim 77, further comprising removing the portions of the at least one metal layer by directional etching.

97. The method of claim 77, further comprising forming the conducting layer from at least one of aluminum and copper.

98. The method of claim 77, comprising forming the metal layer, metal spacer, and upper metal layer of the same metal.

99. The method of claim 98, wherein the metal is Ti.

ABSTRACT OF THE DISCLOSURE

The present invention provides a metallization structure for semiconductor device interconnects such as a conductive line, and methods for making the same, wherein the metallization structure includes a substrate with a substantially planar upper surface, a foundation metal layer disposed on a portion of the substrate upper surface, a primary conducting metal layer overlying the base metal layer, and a metal spacer on the sidewalls of the primary conducting metal layer and the foundation metal layer. The present invention also provides a metallization structure, and a method for making the same, wherein the metallization structure includes a substrate with a foundation metal layer disposed thereon, a dielectric layer with an aperture therethrough being disposed on the substrate, where the bottom of the aperture exposes the foundation metal layer of the substrate and a metal spacer on the sidewall of the aperture and a line or plug of a primary conducting metal fill the remaining portion of the aperture. These metallization structures are useful for reducing the incidence and severity of thermally-induced stress voids.

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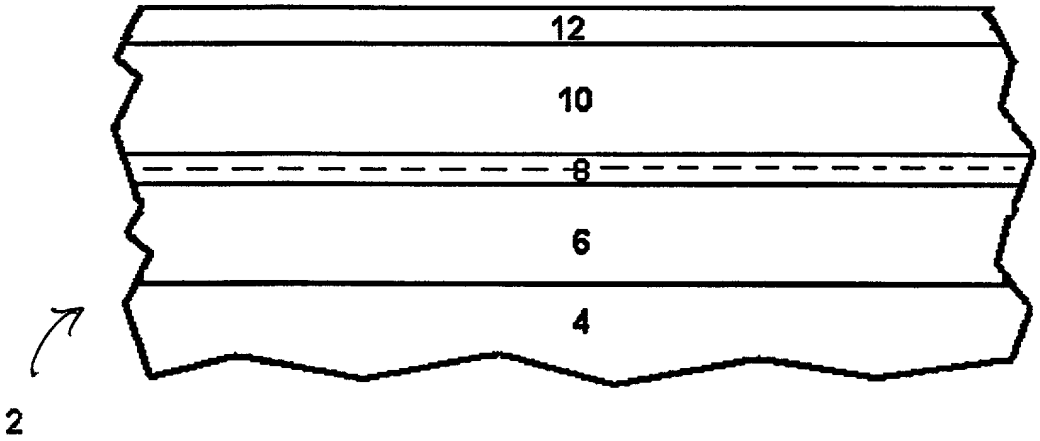
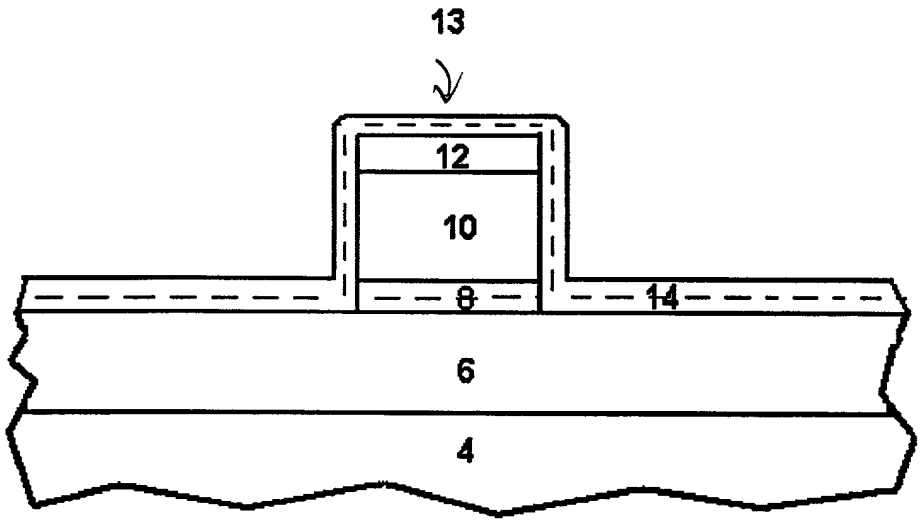


Figure 1



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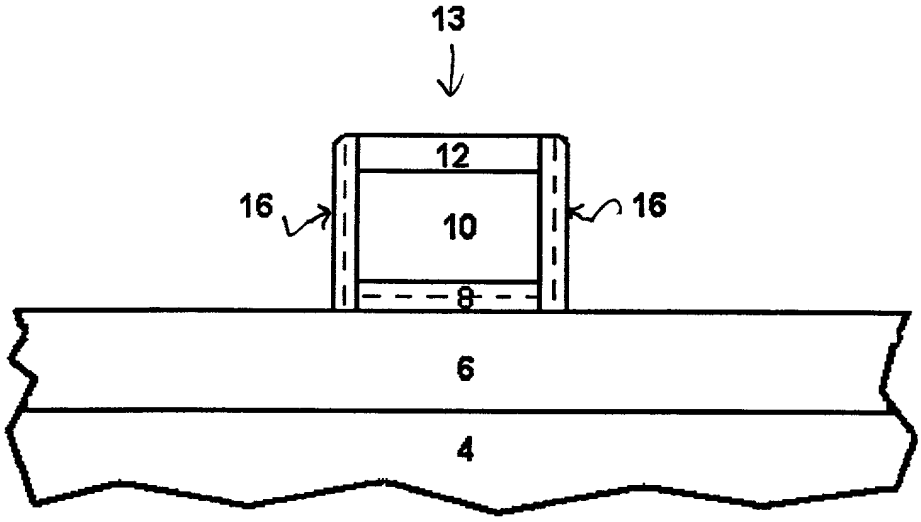


Figure 3a

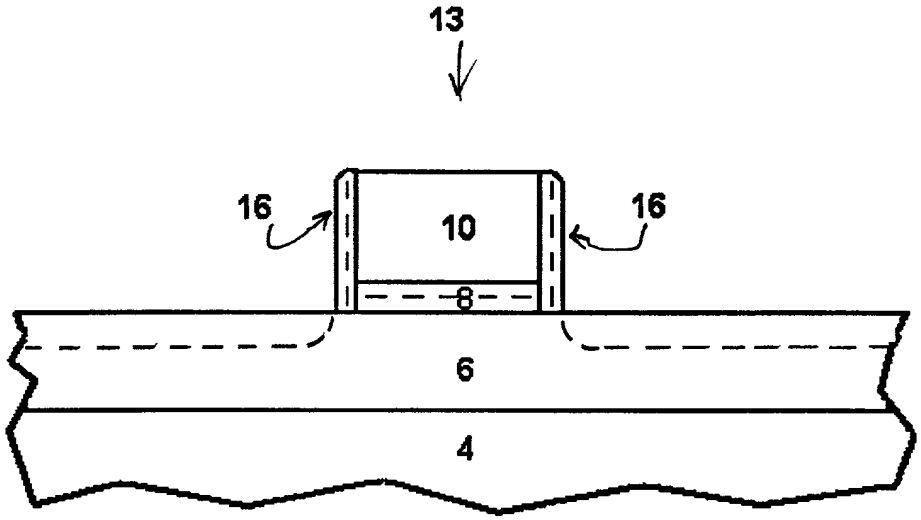
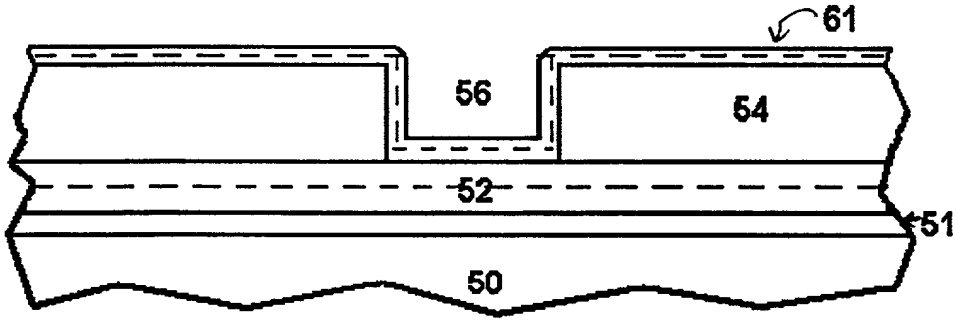


Figure 3b



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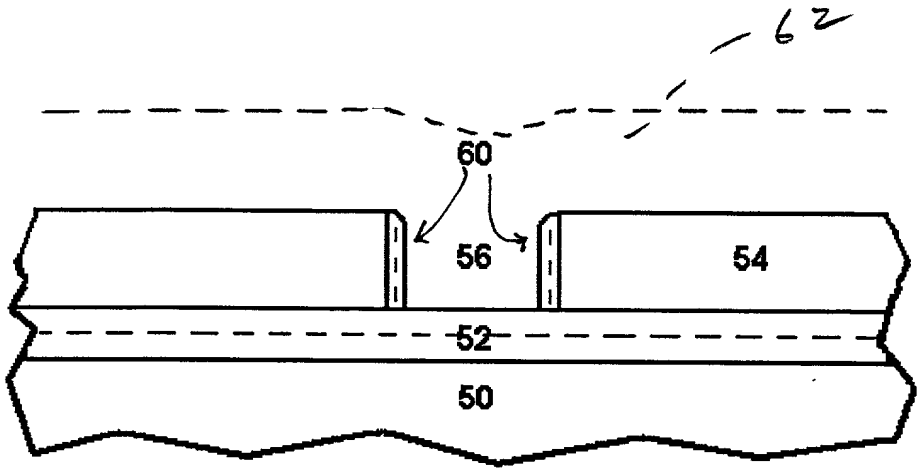

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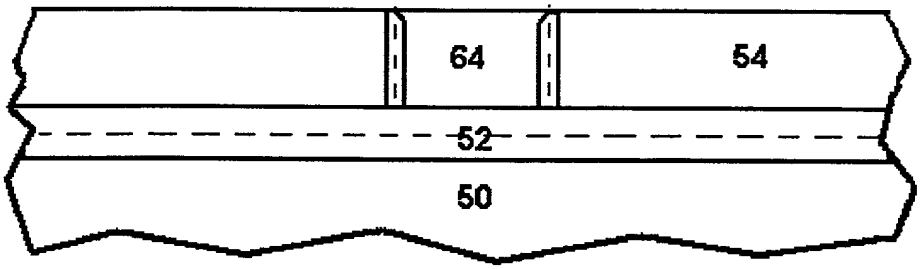

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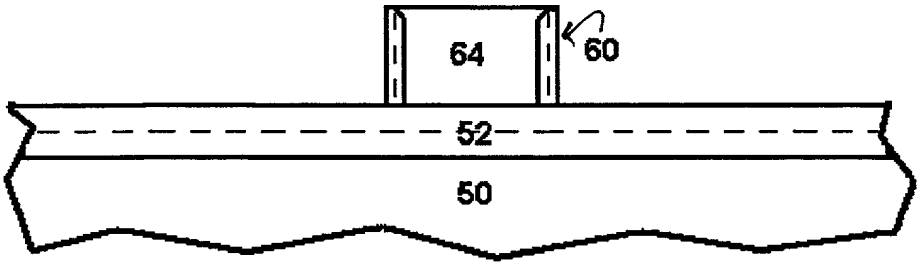

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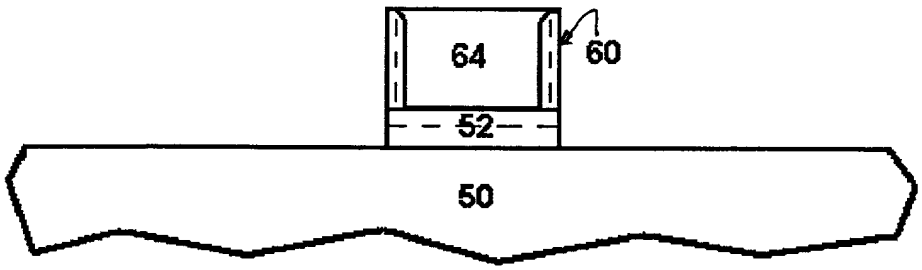
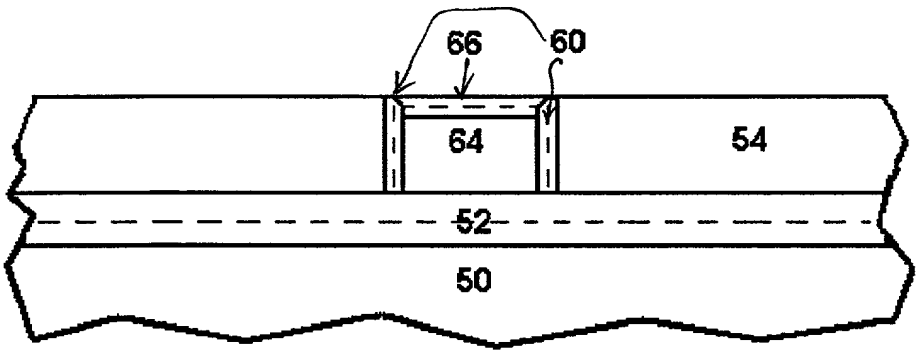


Figure 7b



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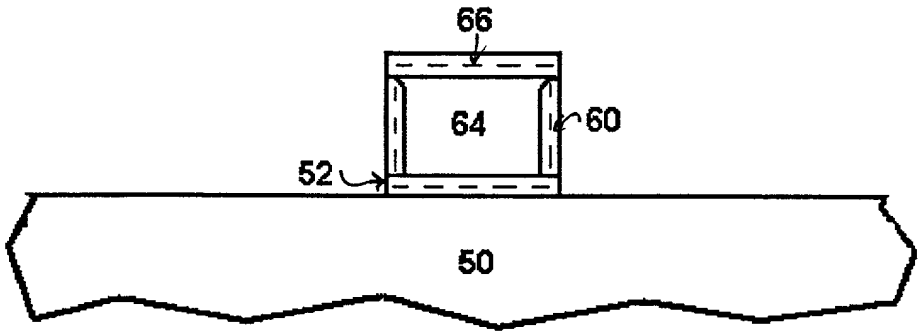

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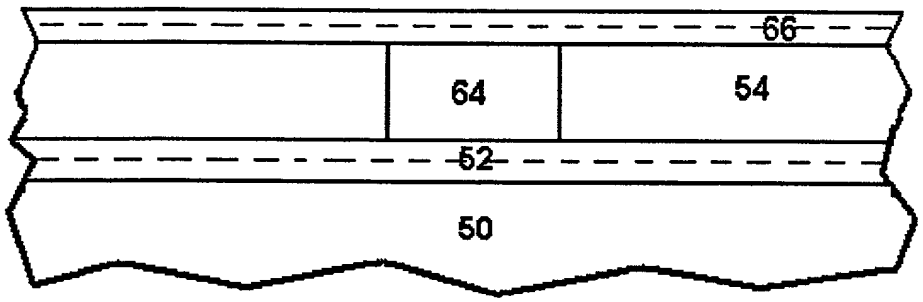

Figure 10

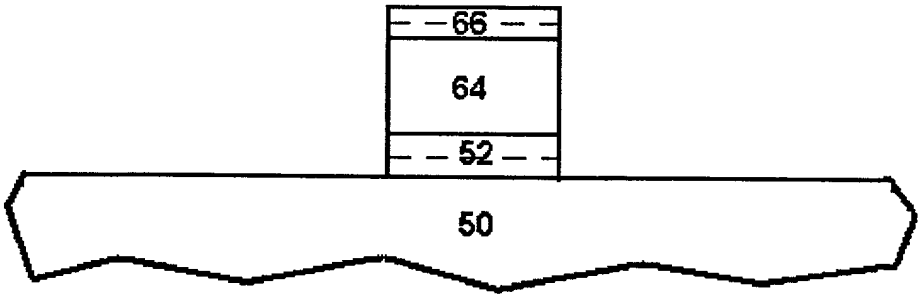

Figure 11

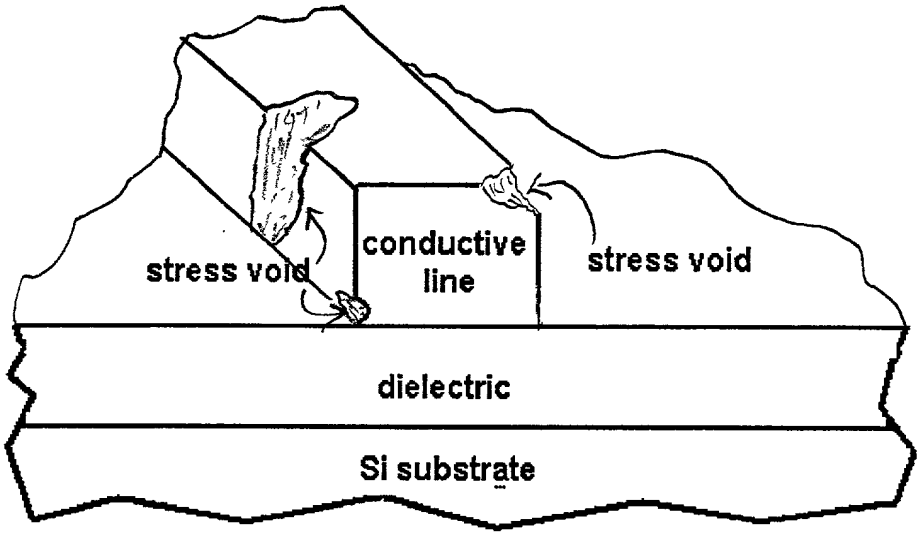

Figure 12
Prior Art

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME , the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
Laurence B. Bond, Reg. No. 30,549
Allen C. Turner, Reg. No. 33,041
Stephen R. Christian, Reg. No. 32,687
Paul C. Oestreich, Reg. No. P-44,983
Kenneth C. Booth, Reg. No. 42,342
Lia M. Pappas, Reg. No. 34,095
William S. Britt, Reg. No. 20,969
Joseph A. Walkowski, Reg. No. 28,765
Kent S. Burningham, Reg. No. 30,453
Brick G. Power, Reg. No. 38,581
Devin R. Jensen, Reg. No. P-44,805
Samuel E. Webb, Reg. No. 44,394
Thomas J. Rossa, Reg. No. 26,799
James R. Duzan, Reg. No. 28,393
Edgar R. Cataxinos, Reg. No. 39,931
Kenneth B. Ludwig, Reg. No. 42,814
Eleanor V. Goodall, Reg. No. 35,162
Michael L. Lynch, Reg. No. 30,871

Address all correspondence to: Joseph A. Walkowski, telephone no. (801) 532-1922.
TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Salman Akram
Inventor's signature Salman Akram Date August 31st 1999
Residence: Boise, Idaho
Citizenship: Pakistan
Post Office Address: 1463 E. Regatta, Boise, Idaho 83706

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Salman Akram	**Examiner:**	Unknown
Serial No.:	Not Yet Assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	3442US (96-428)
Title:	METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME		

POWER OF ATTORNEY BY ASSIGNEE
AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R. Christian, Reg. No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C. Oestreich, Reg. No. P-44,983	Devin R. Jensen, Reg. No. P-44,805	Eleanor V. Goodall, Reg. No. 35,162
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	Michael L. Lynch, Reg. No. 30,871
Lia M. Pappas, Reg. No. 34,095		

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

[] In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

[X] In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

Joseph A. Walkowski,
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, UT 84110
Tele: (801) 532-1922
Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC.

Date: Aug 31, 1999

By: _____
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.

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